

G41T-M

Ver. 7.1

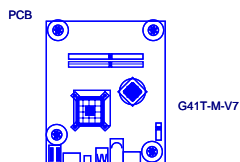
History :

06/26 -> Version A release.

08/11 -> 1.0 Release
P09. Modify ER38 from 24.9 ohm to 30.1ohm for SATA signal.
P27. Modufy ER68, ER69, ER73, C153 to larger value for fix S3 wake up in-rush current issue.
P29. Fixschematic ISP, ISN error issue.
P29. Modify damping resister to 2.2 ohm and del VIN MLCC.

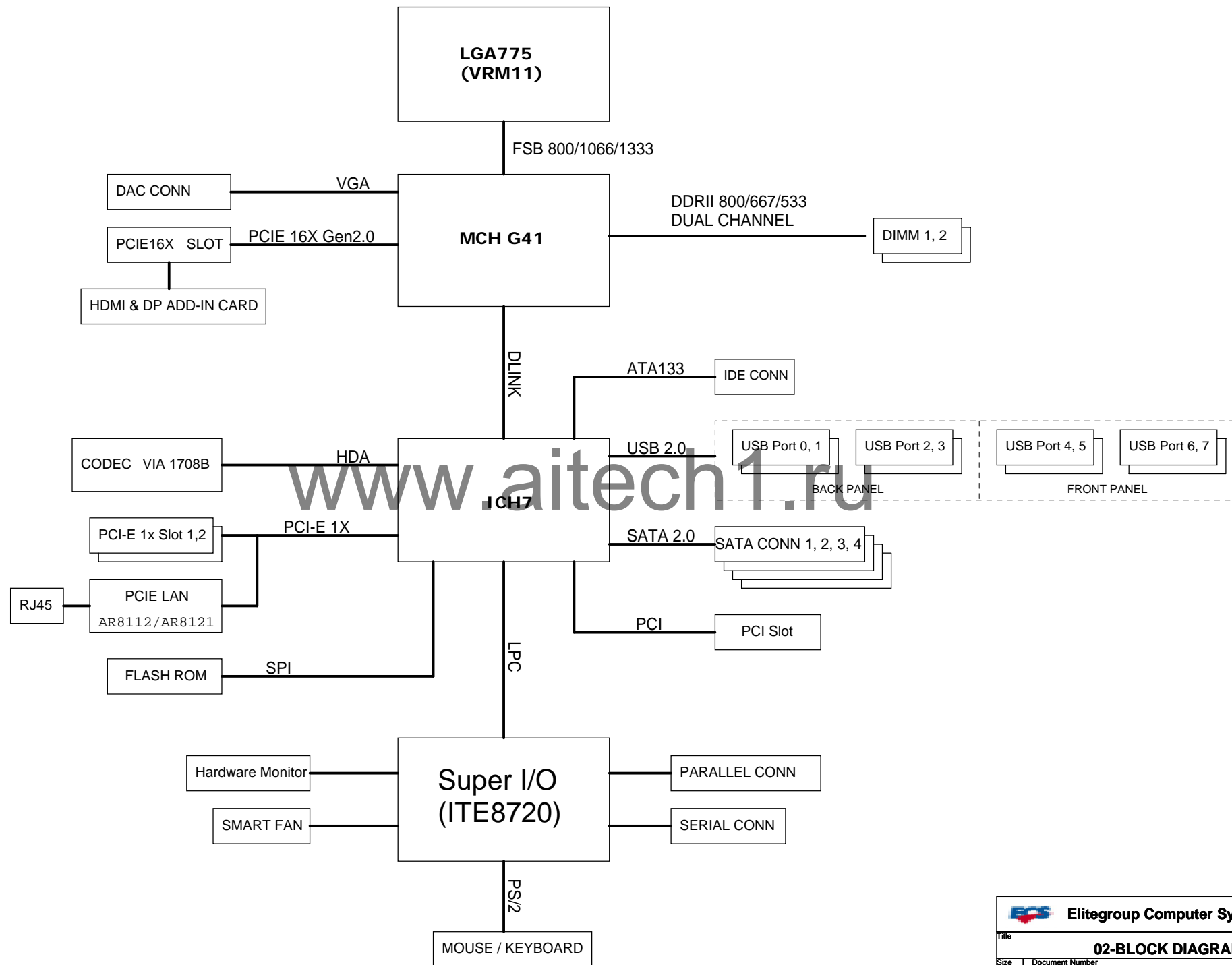
09/08 -> 1.0A Release
P23. Remove RN43,44,45 LPT damping resisters
P23. Connectot SB THERM- to SIO GPIO to tupport Shutdown Temperature
P30. Connectting ATX_PWRGD to P23 SIO.95pin

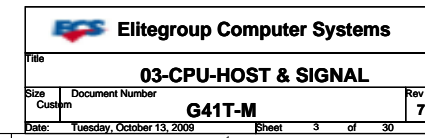
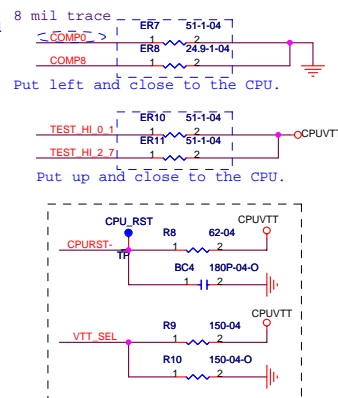
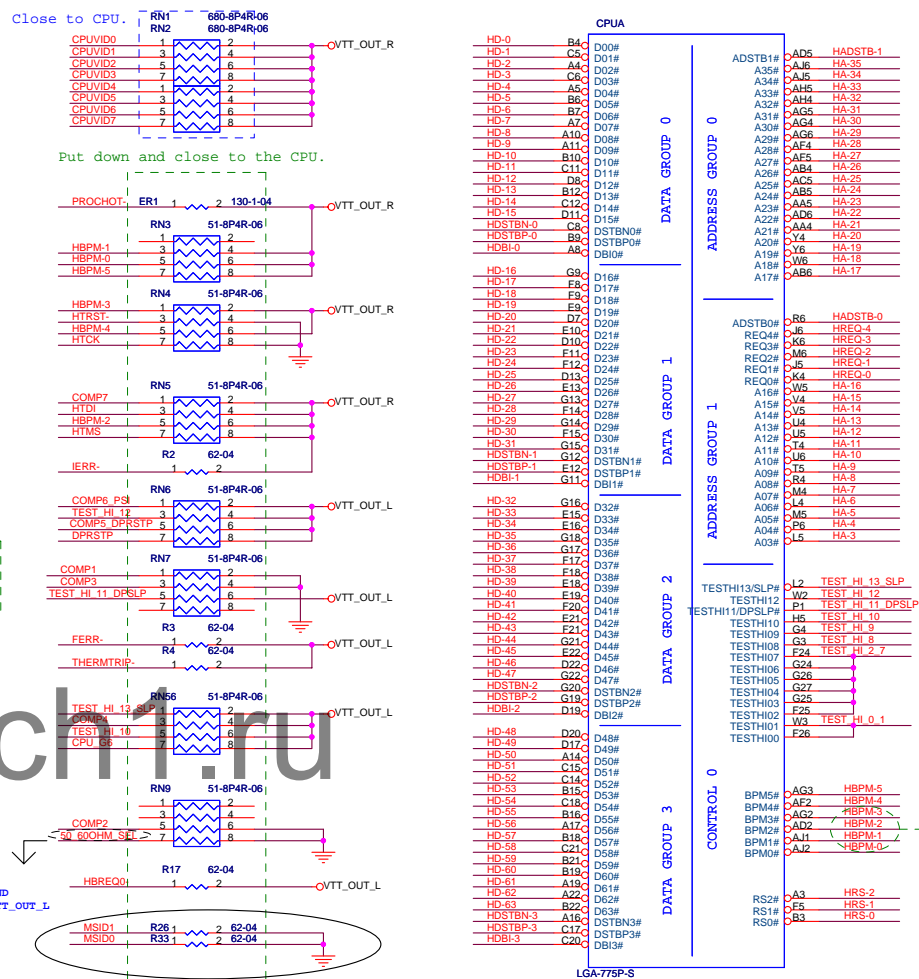
10/02 -> 1.9 Release
P29. Modify VCORE MOS to up1-down2 to support 95W CPU

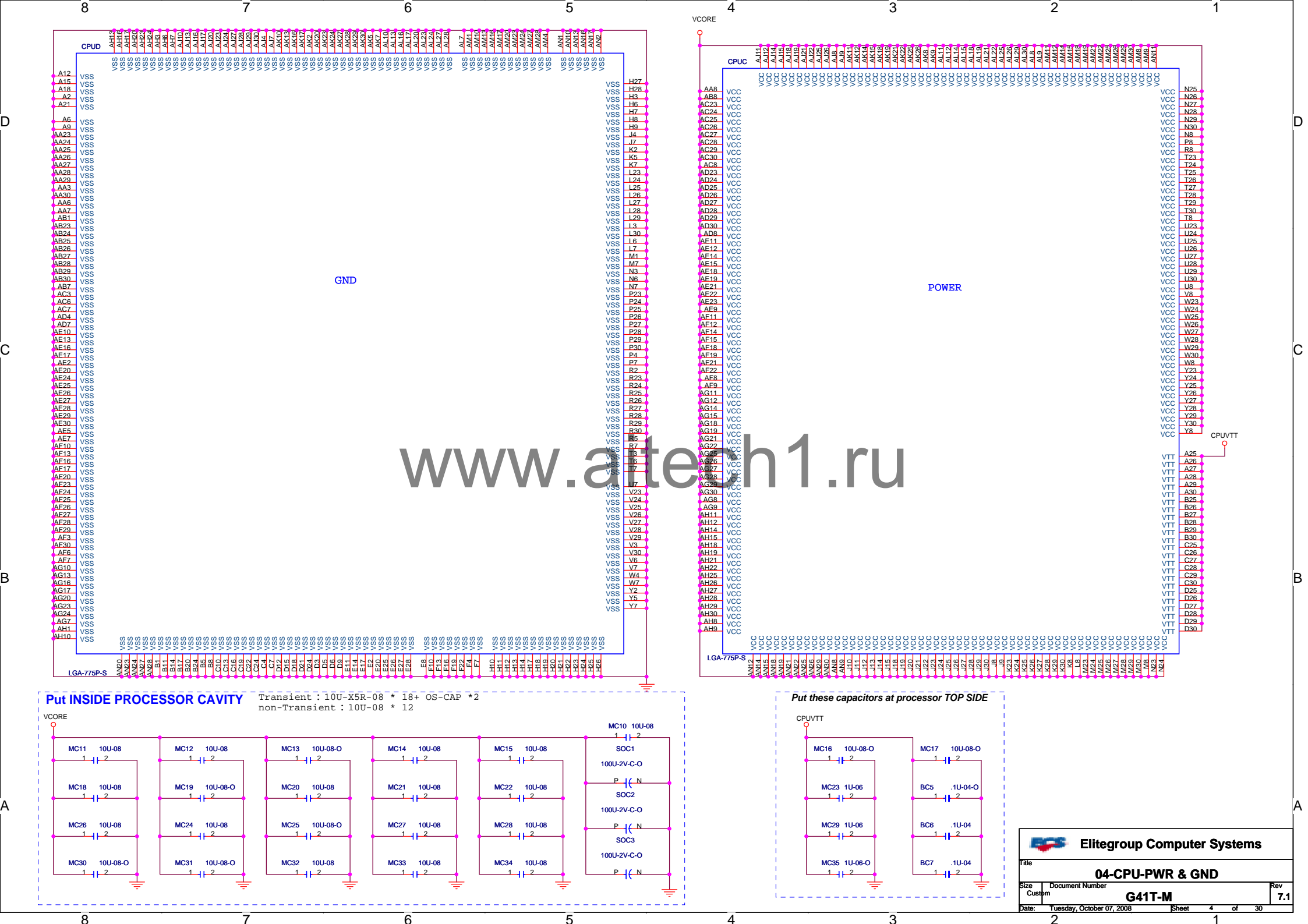


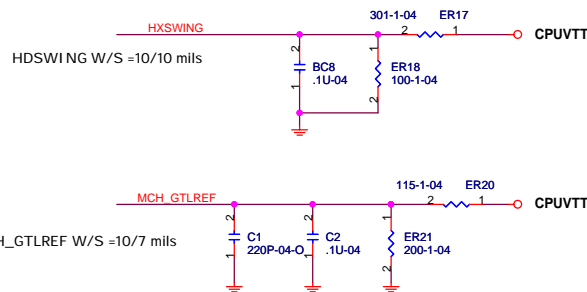
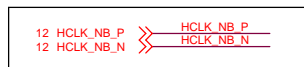
Page Index

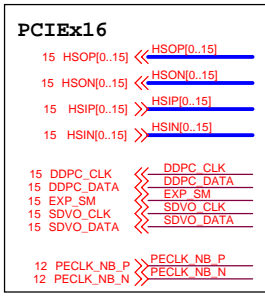
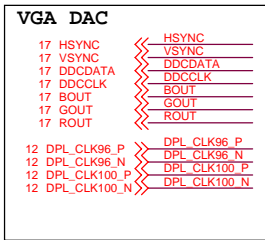
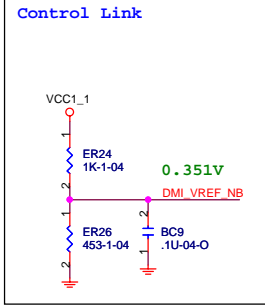
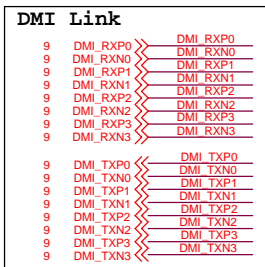
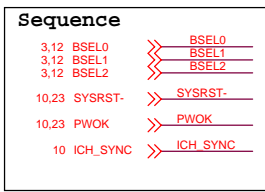
01-COVER PAGE
02-BLOCK DIAGRAM
03-CPU-HOST & SIGNAL
04-CPU-PWR & GND
05-MCH-HOST
06-MCH-DMI/PCIE/DAC/HDMI
07-MCH-MEMORY
08-MCH-PWR/GND
09-ICH7-DMI/PCIE/SATA/USB/MISC1
10-ICH7-HDA/RGMII/SPI/PCI/RTC/MISC2
11-ICH7-PWR/GND
12-CLK GEN ICS9LPRS926
13-DDR2 DIMM1,2
14-DDR TERMINATION
15-PCIE 16x/1x Slot
16-PCI Slot
17-VGA (RGB)
18-USB
19-PCIE LAN (RTL8111DL/8103EL)
20-Audio Codec (VIA 1708B)
21-Audio Interface (3 Port HDA)
22-BOM 104 Level
23-Super I/O (ITE 8713)
24-KB / MS / FDD /HOLE
25-COM / LPT
26-HM / Fan / Ring / IR
27-Voltage Regulator
28-Dual Power
29-VRD11.1 (Richtek 8857)
30-ATX / PANEL











For G41 Only :

CL_CLK and CL_DATA No Connect

CL_RST# Connect to PLTRST#

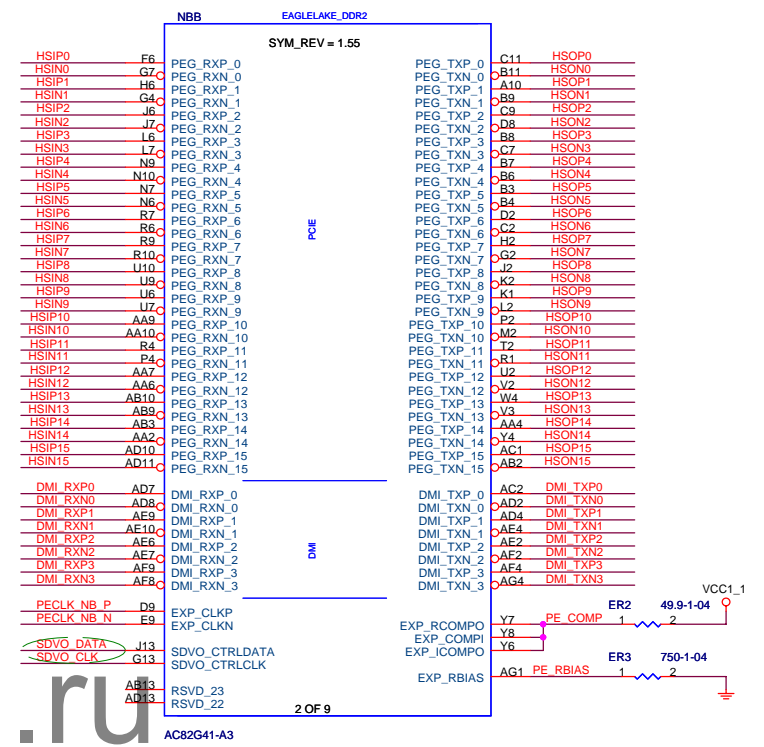
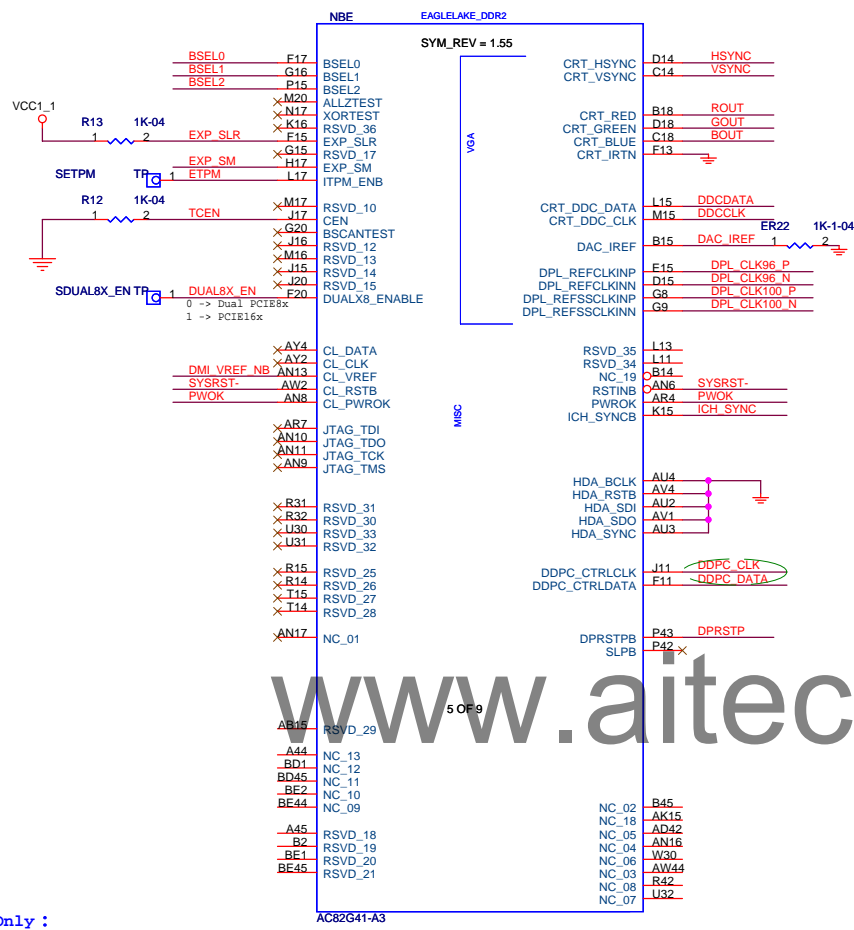
CL_VREF achieve 0.352 reference voltage

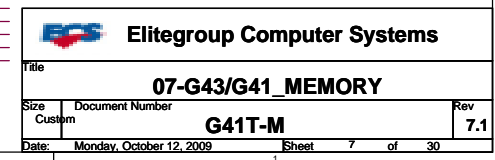
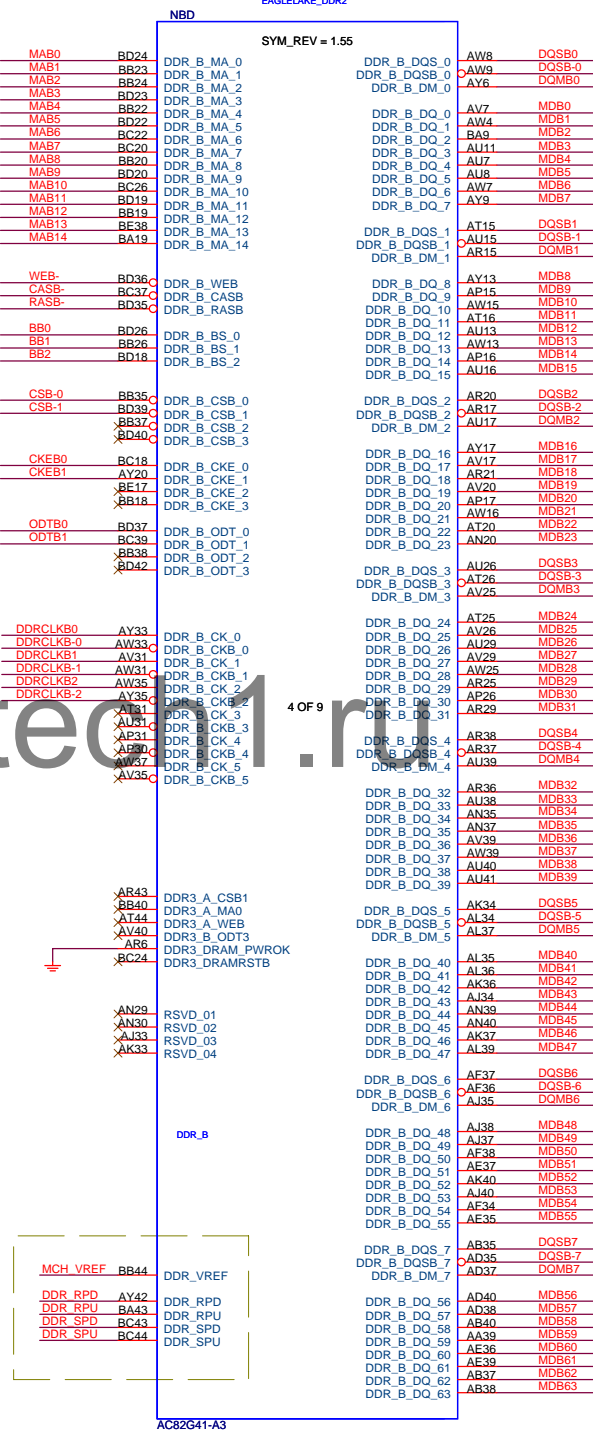
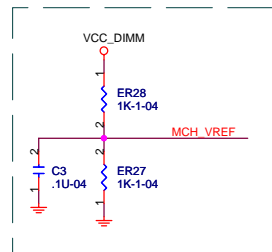
CL_PWROK Connect to PWOK

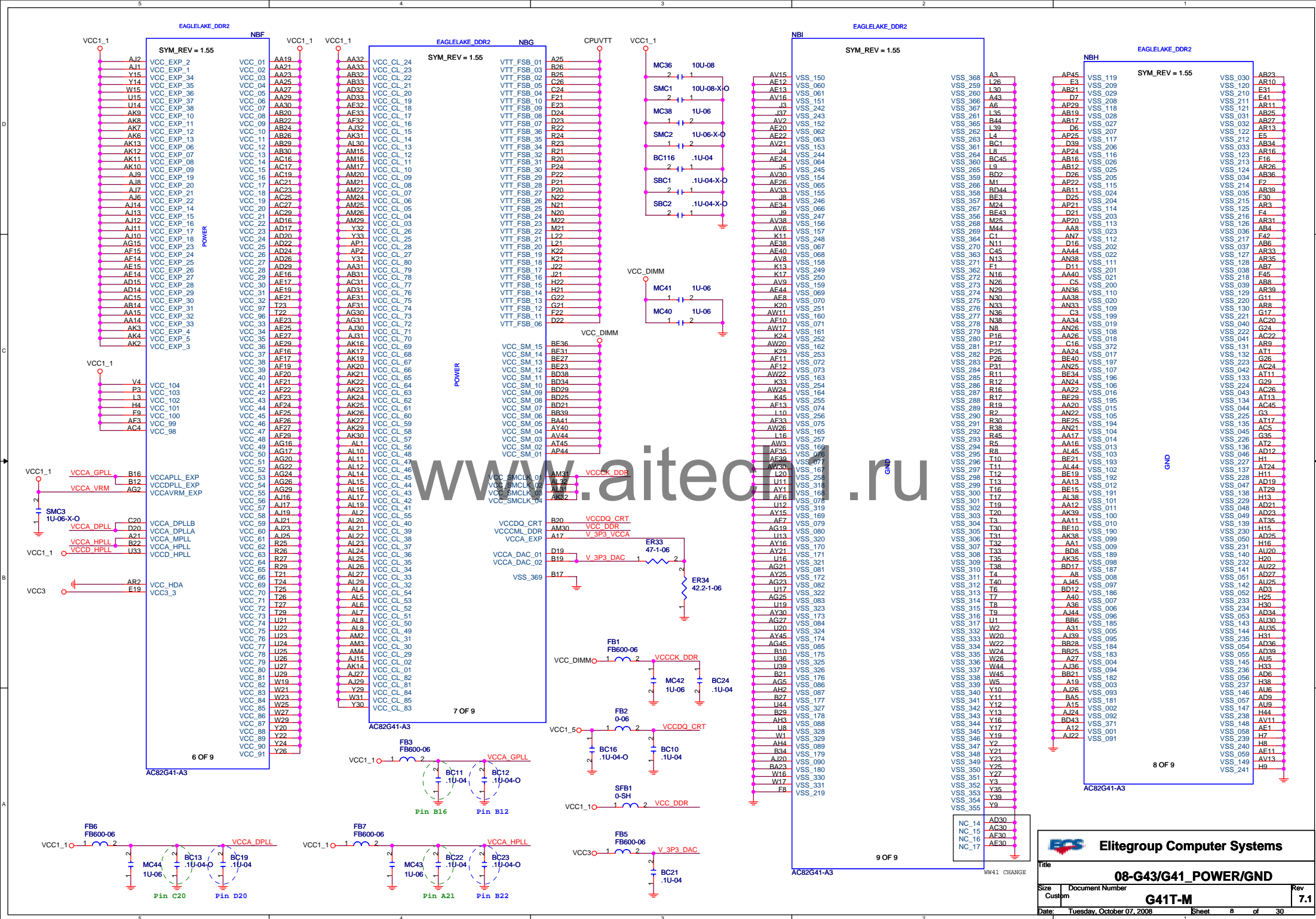
VCC_CL Connect to 1.1V GMCH core voltage

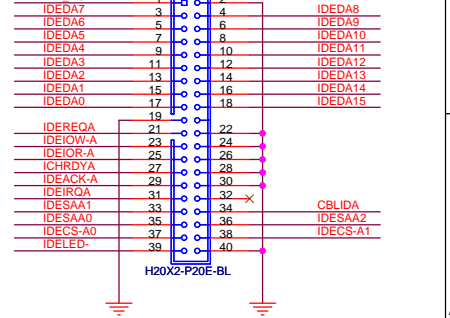
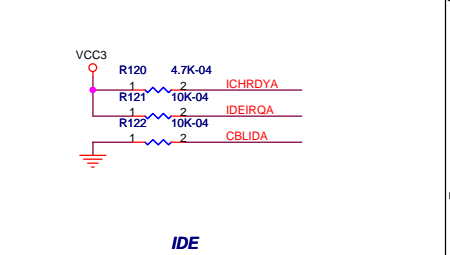
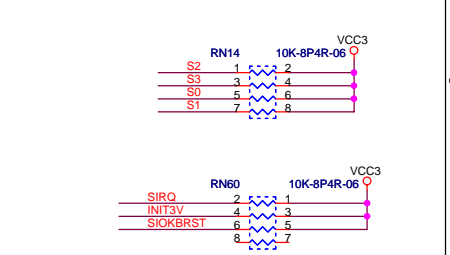
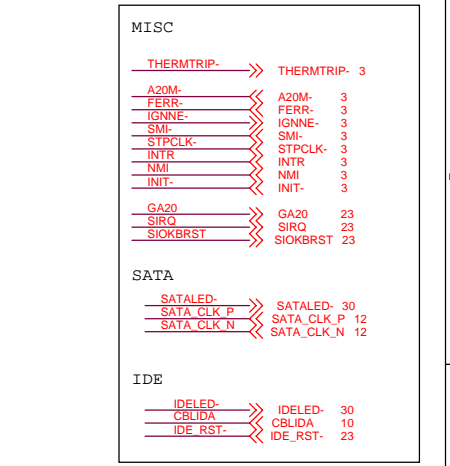
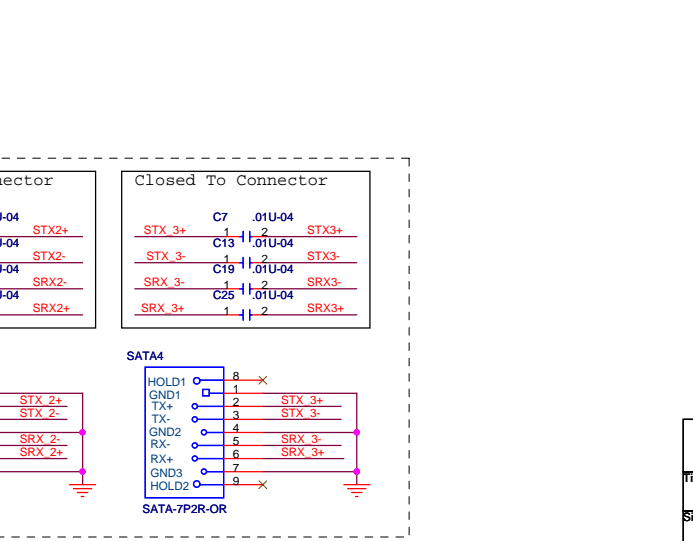
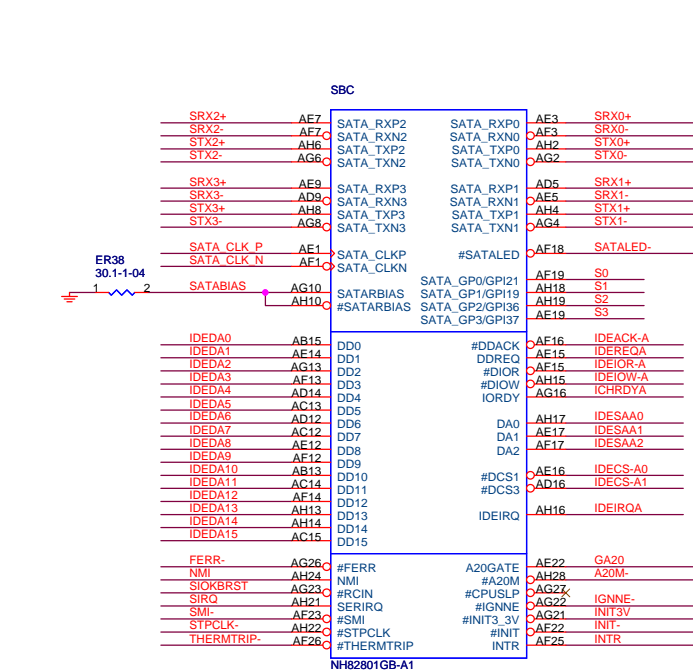
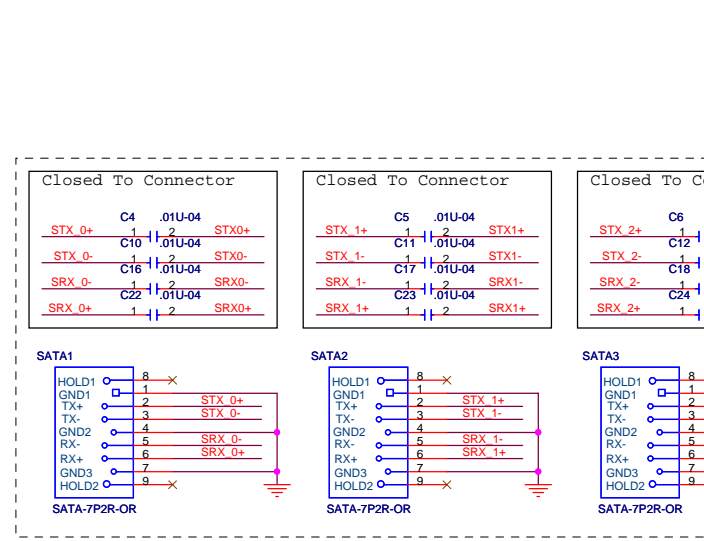
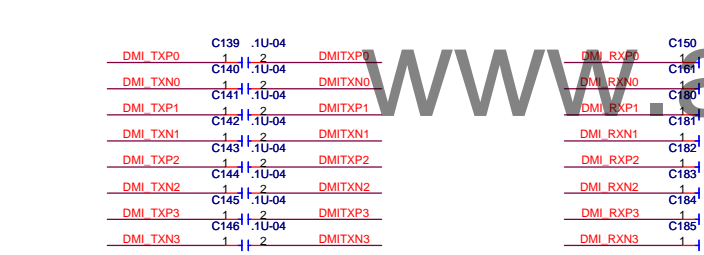
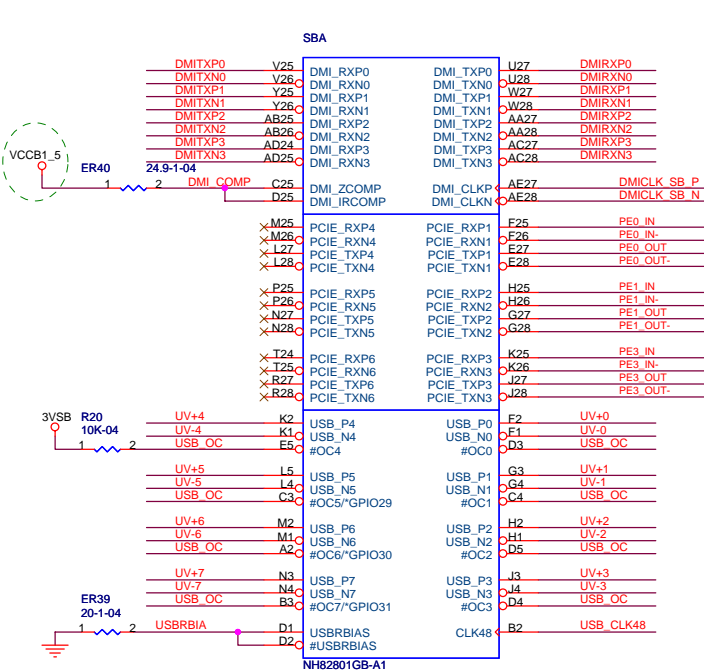
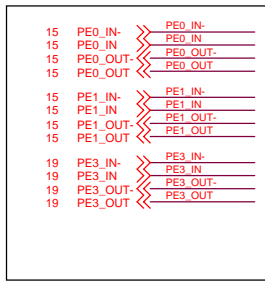
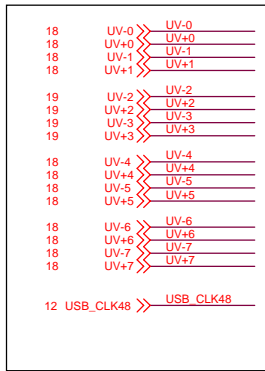
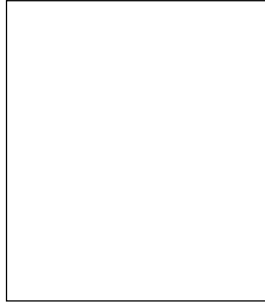
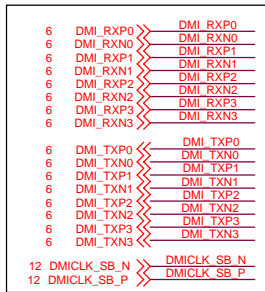
TPM1.2 STRAPS TABLE			
	ENABLE	DISABLE	DESCRIPTION
ETPM	L	Floating	TPM1.2 on MCH In MCH Pin.L17
SPIDO	H	Floating	TPM1.2 on ICH10 In ICH10 Pin.C26
TPM_PP	H	L	TPM Physical Presence In ICH Pin.C12

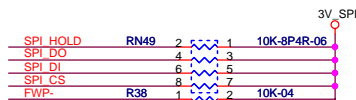
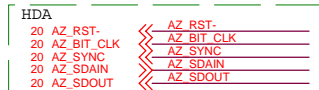
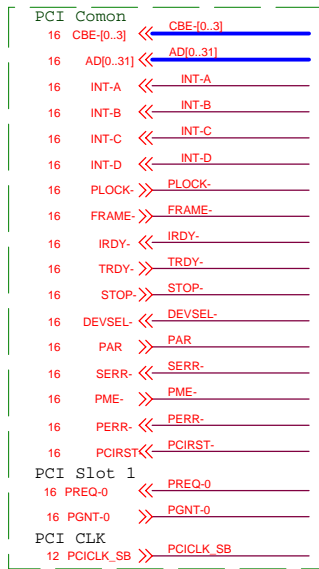
GMCH STRAPS TABLE			
	H	L	DESCRIPTION
EXP_SLR	NORMAL/ ATX	REVERSE/ BTX	PCI EXPRESS STATIC LANE REVERSAL
EXP_SM	CONCURRENT	NON-CONCURRENT	PCI EXPRESS / SDVO COEXISTENCE
TCEN	ENABLE	DISABLE	TLS CONFIDENTIALITY



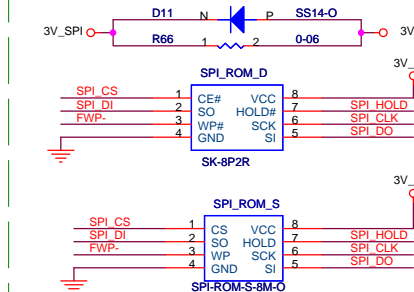




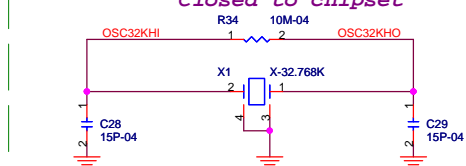




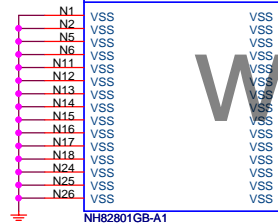
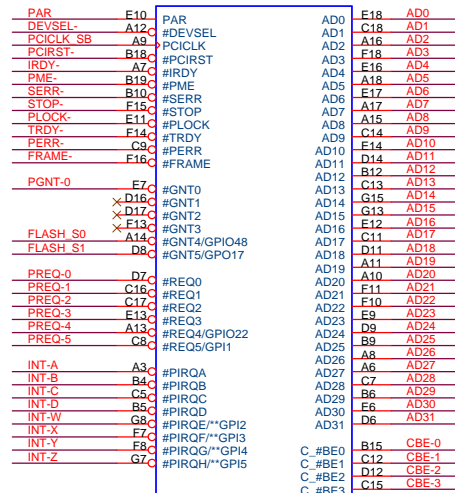
SPI ROM



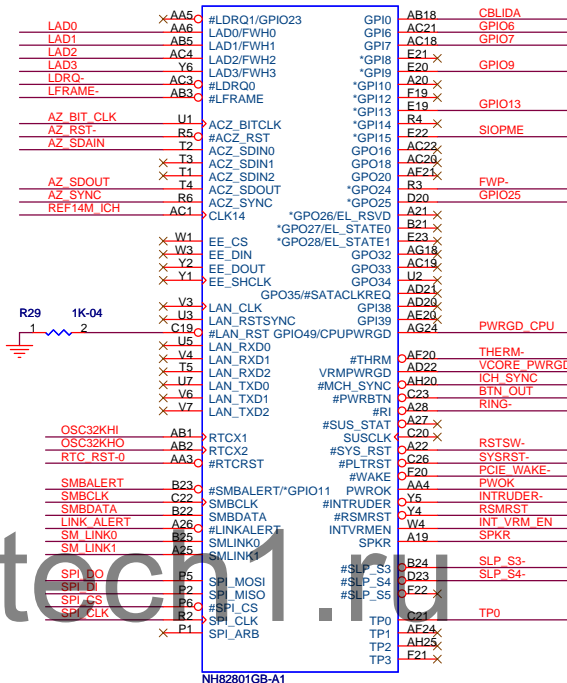
RTC CLK



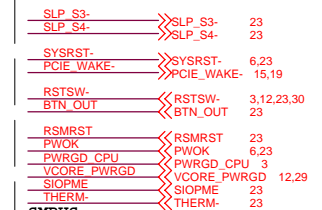
SBB



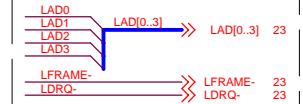
SBD



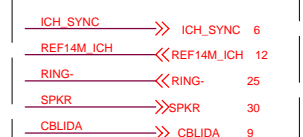
ACPI



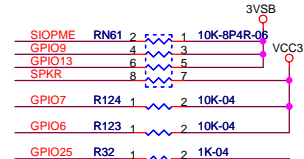
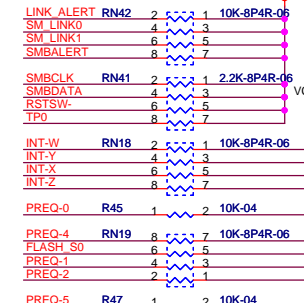
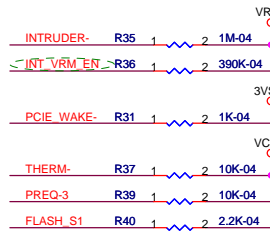
LPC



Others



Strap to Enable Internal SUS VRM



FLASH_S1	FLASH_S0	Flash Cycle
0	1	SPI
1	0	PCI
1	1	LPC

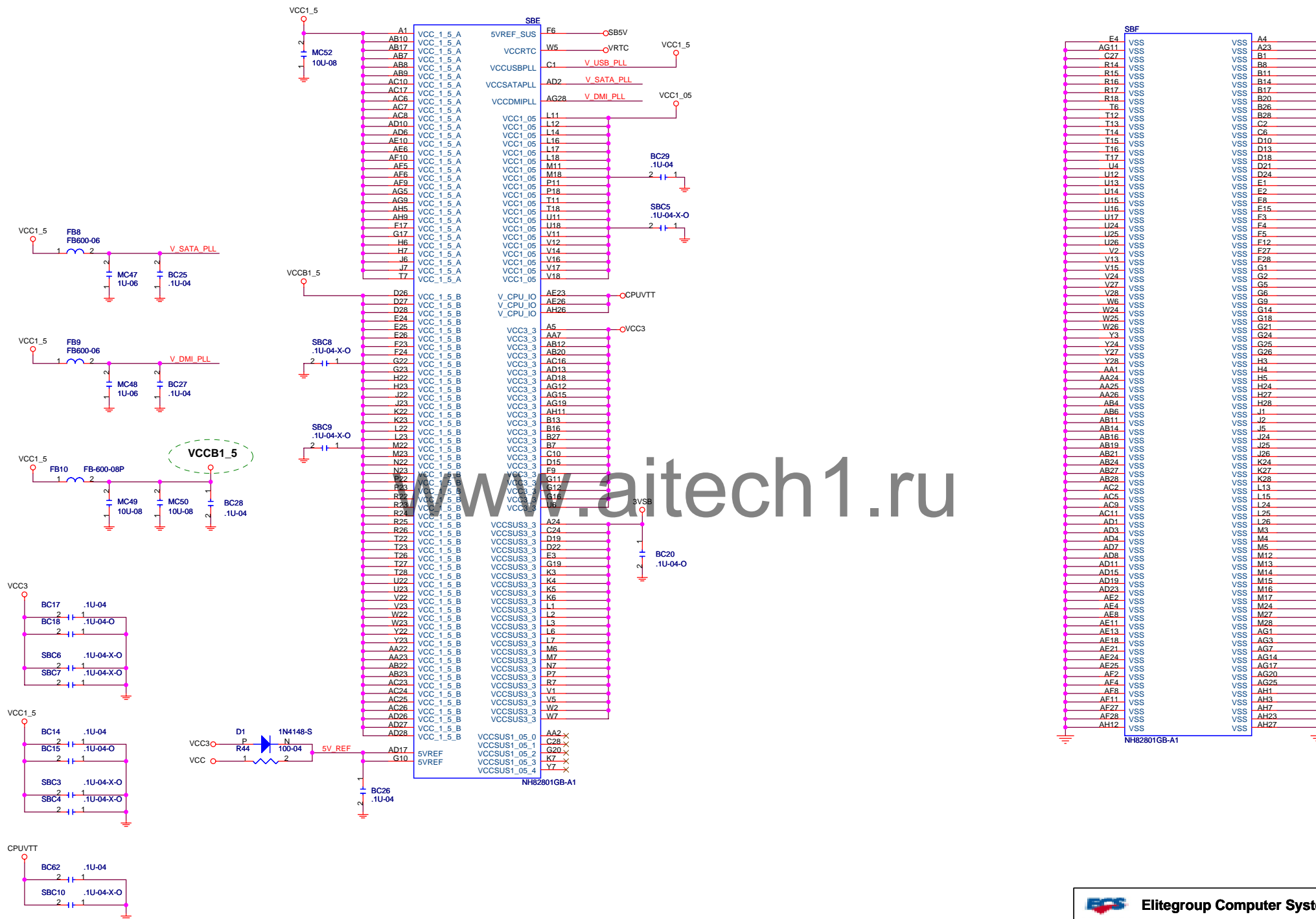
	H	Floating	DESCRIPTION
AZ_SDOUT	PCIE 4x *1	PCIE 1x *4	PCIE 1x/4x Select
AZ_SYNC	PCIE 4x *1	PCIE 1x *4	PCIE 1x/4x Select

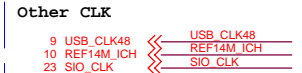
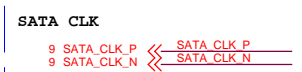
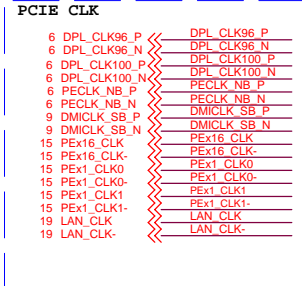
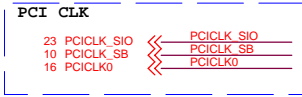
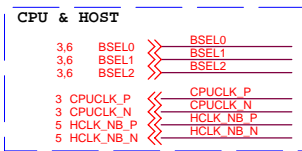
Elitegroup Computer Systems

File: **10-ICH7_HDA/SPI/PCI/RTC/MISC**

Size: Custom Document Number: **G41T-M** Rev: **7.1**

Date: Monday, October 12, 2009 Sheet 10 of 30

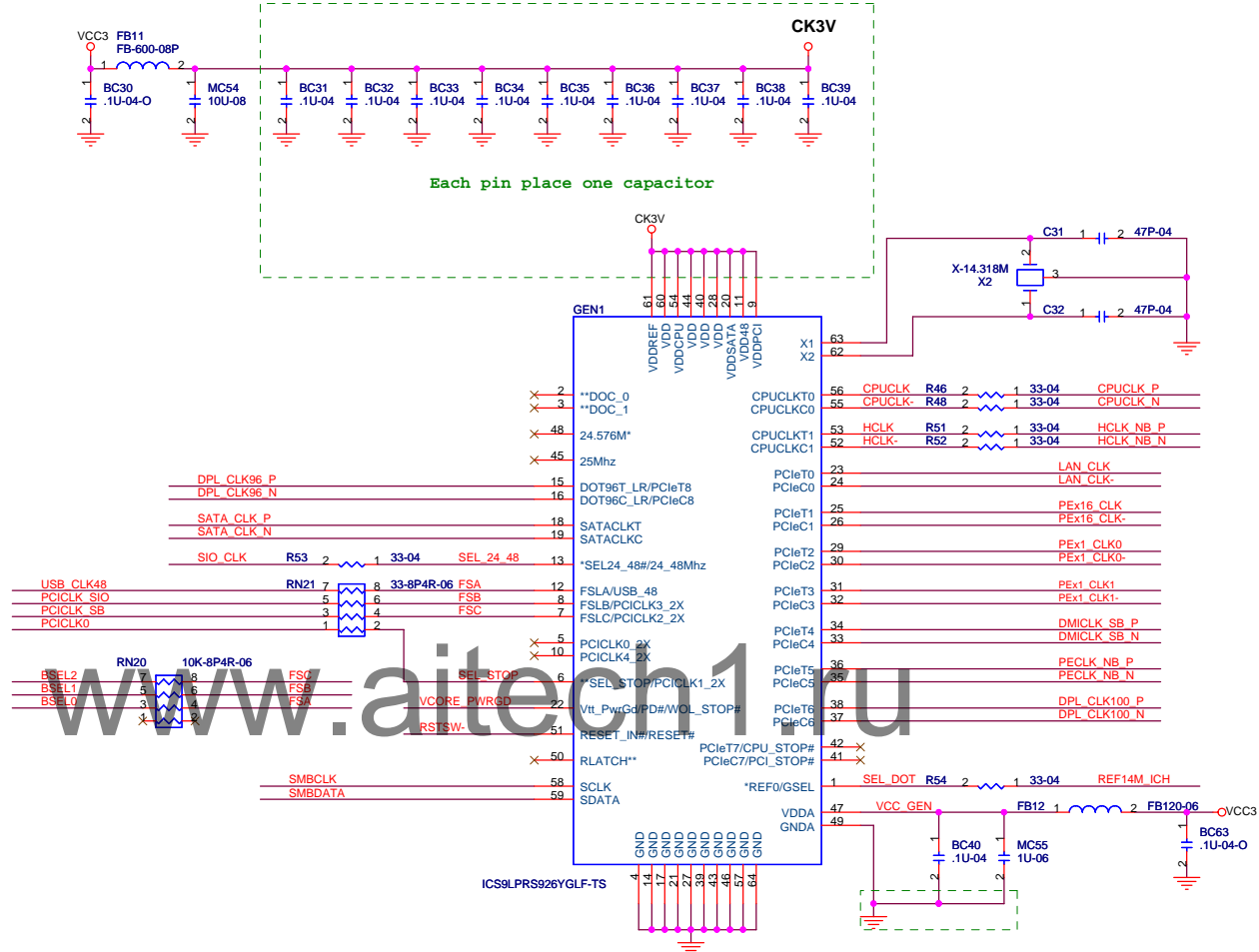
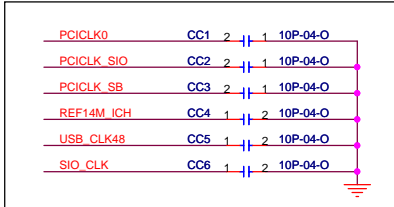
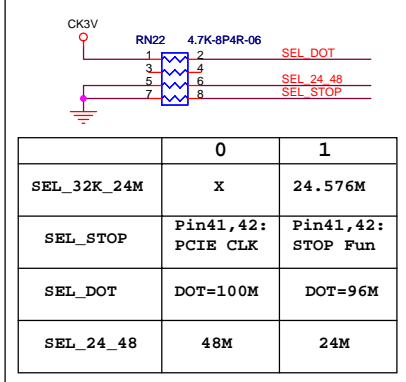


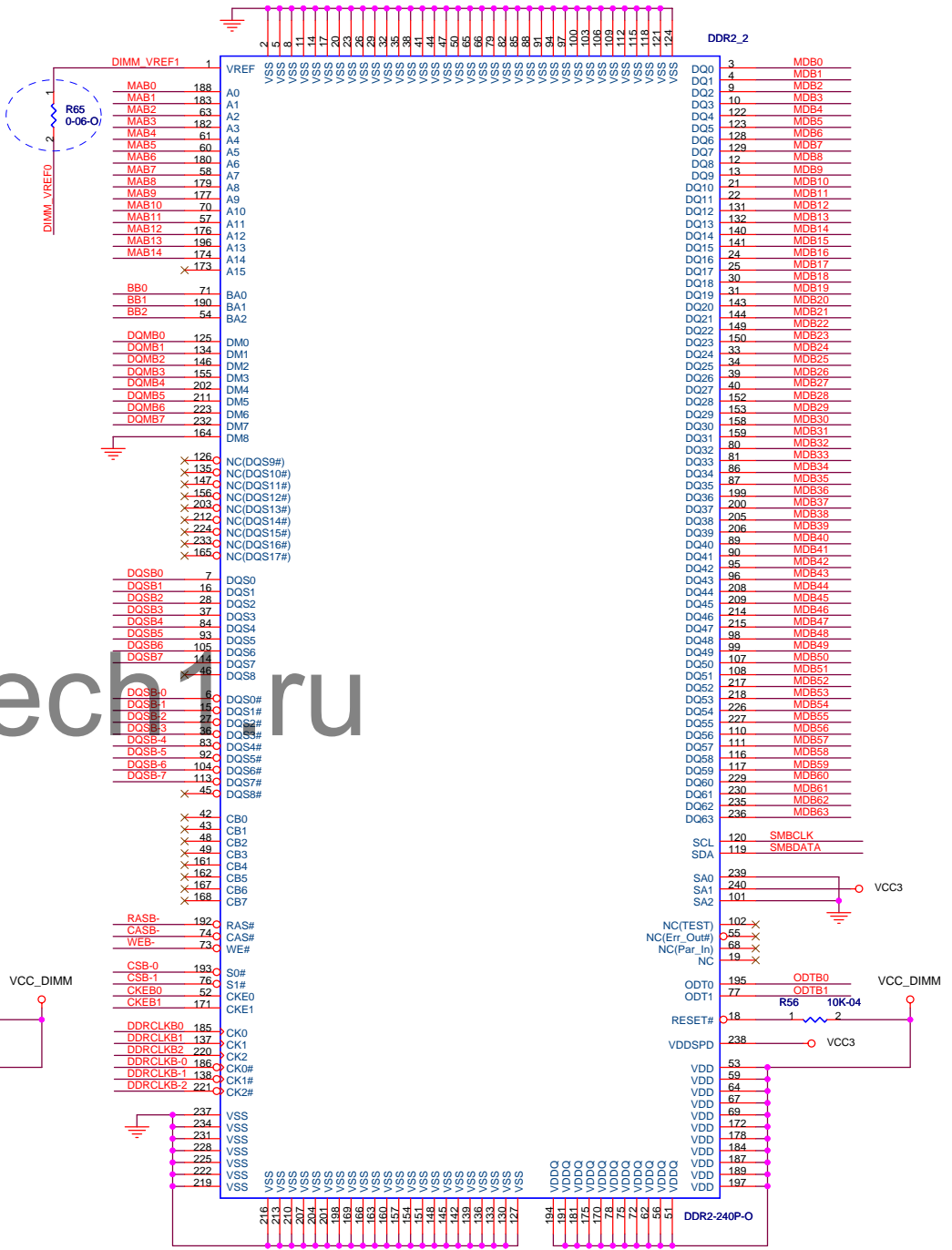
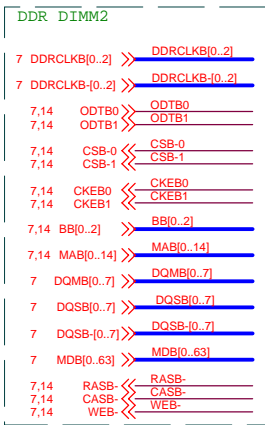
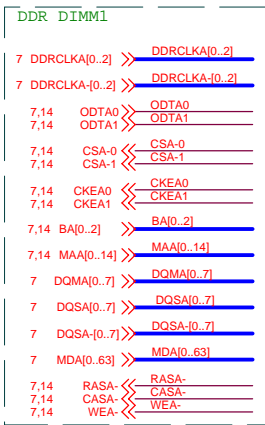
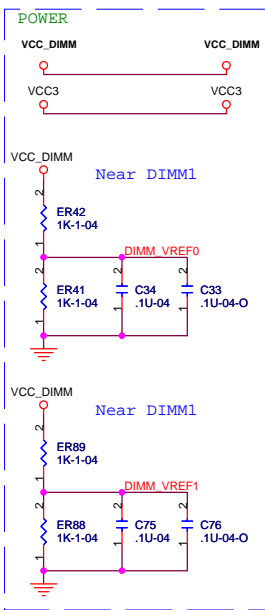


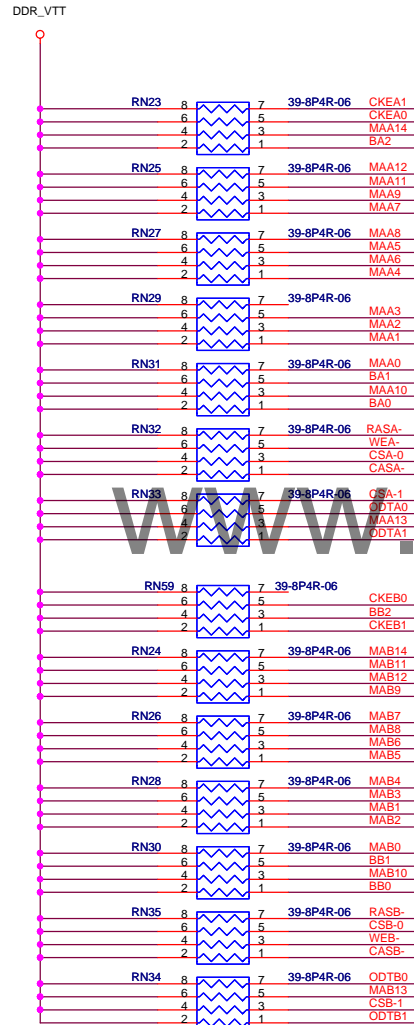
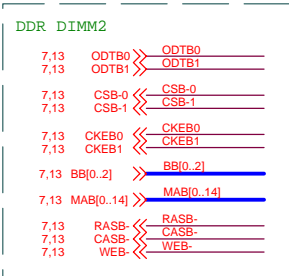
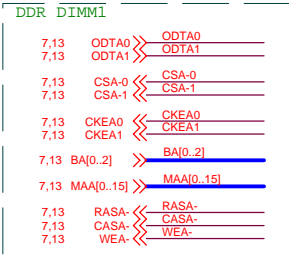
BSEL TABLE

BIT2 FSLC	BIT1 FSLB	BUT0 FSLA	FSB (CPU) FREQ.
0	0	0	266 MHZ (1066)
0	1	0	133 MHZ (800)
1	0	0	333 MHZ (1333)

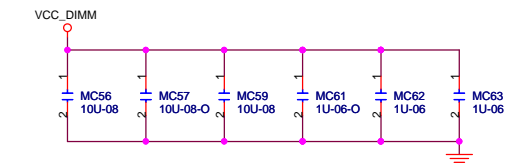
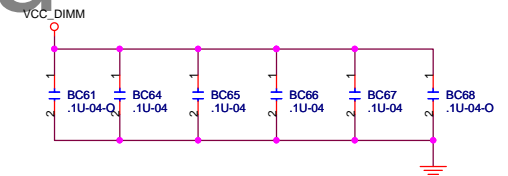
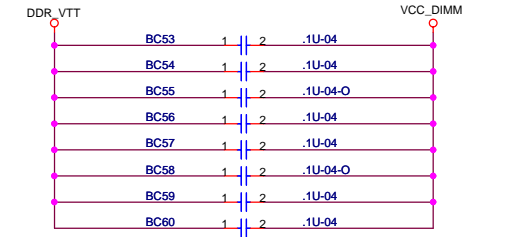
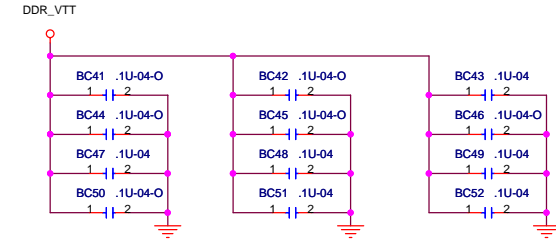
HW Strapping

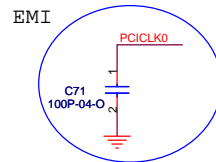
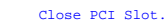
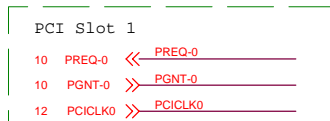




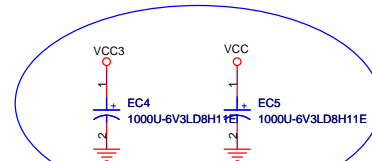


DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND
Placed within 200mils of VTT Termination R-packs

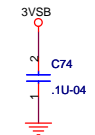
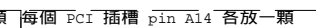
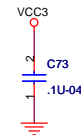
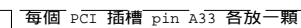
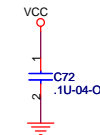
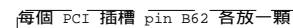
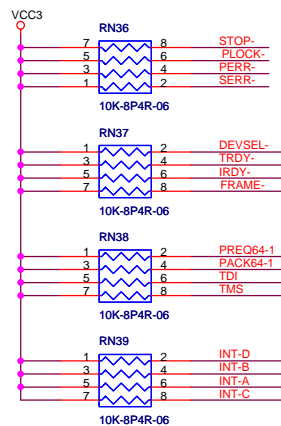


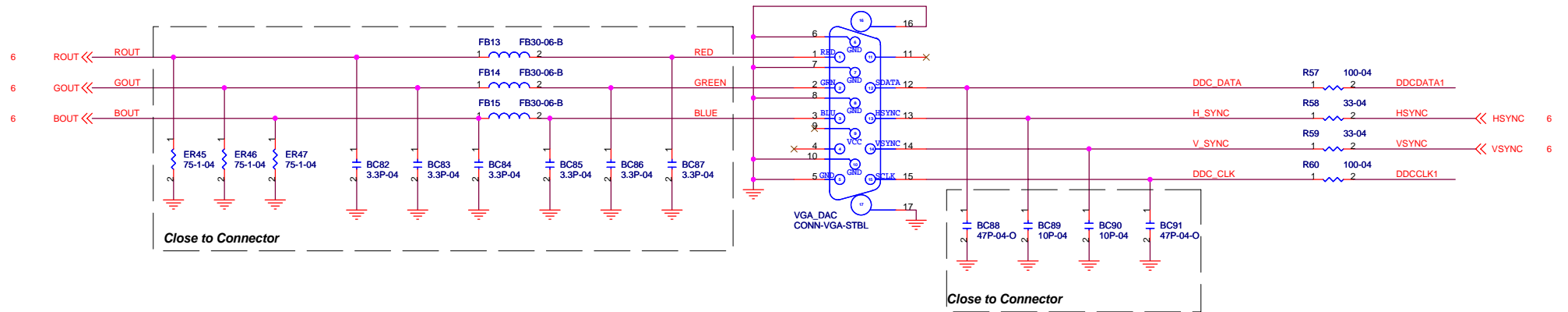


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IDSEL=AD20
INT[A,B,C,D]
```



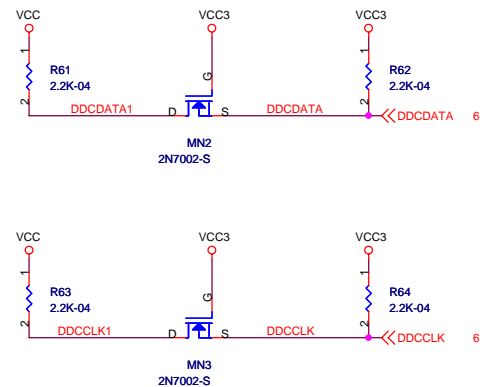
Please place close to PCI1 and PCI2 Slot.



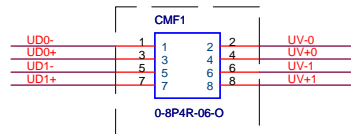
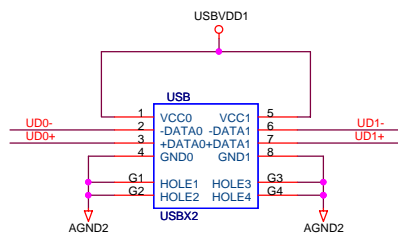
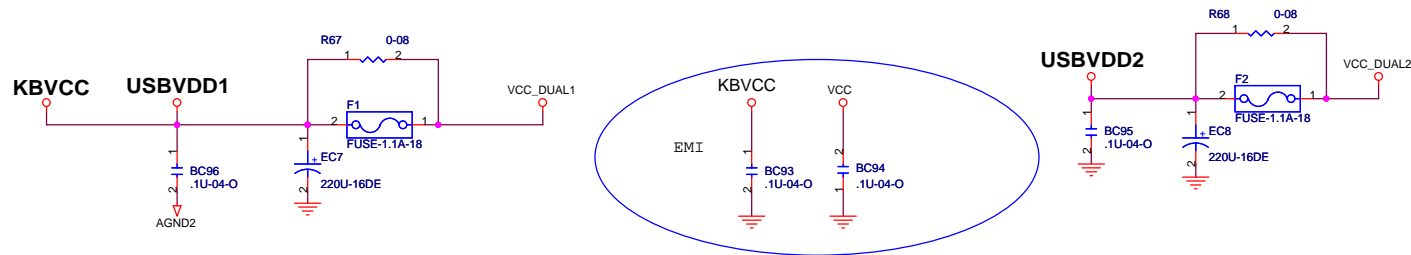
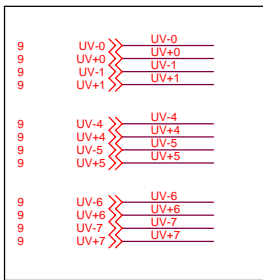


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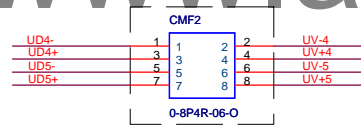
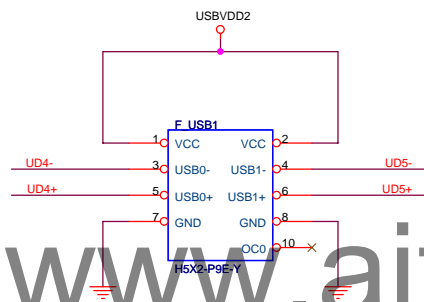
They Can Put Near Connector or Chipset Side, By Placement State



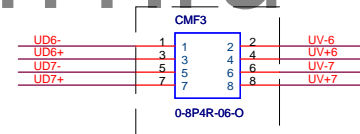
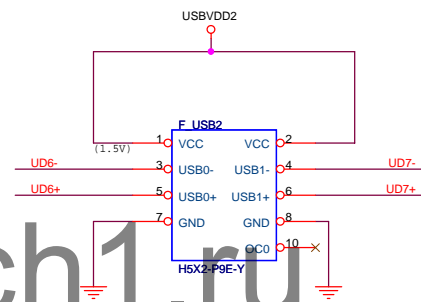
Close to Connector



Close to USB connector

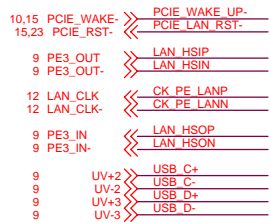


Close to header(F_USB1)



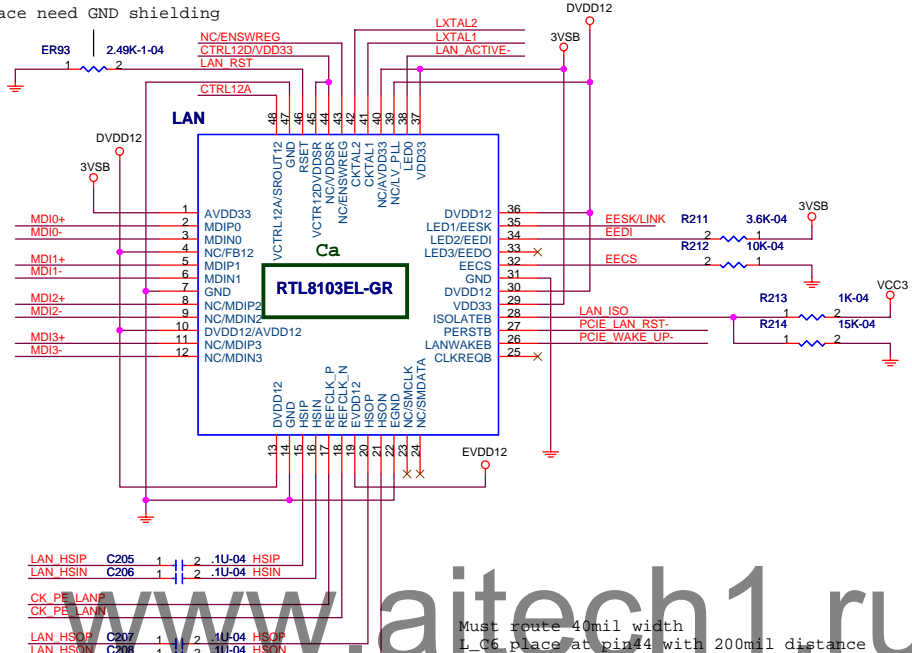
Close to header(F_USB2)

External Connection

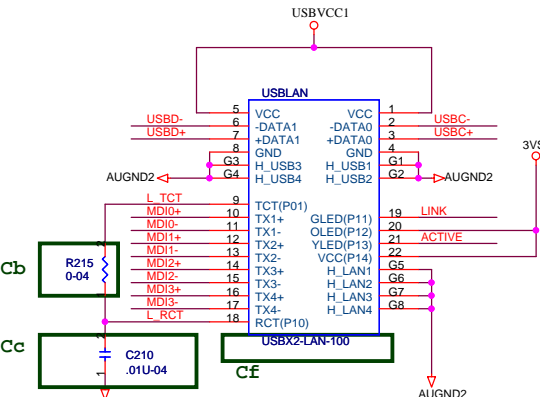
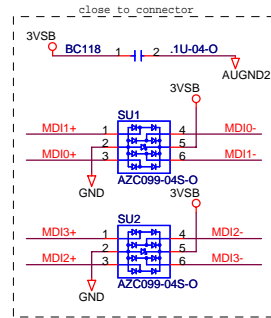
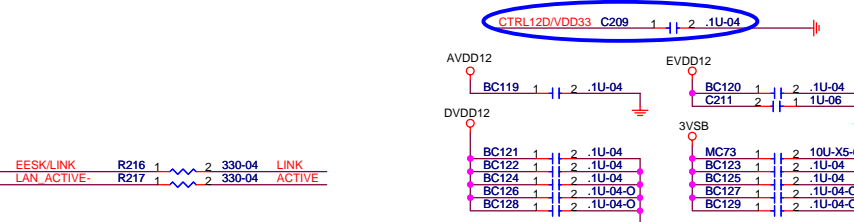


When you found some bug, please inform Ren(ext:665) to update circuit.

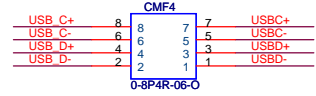
RSET電阻需close to LAN
Trace need GND shielding



Must route 40mil width
L_C6 place at pin44 with 200mil distance



Link: Green on
Active: Yellow blinking



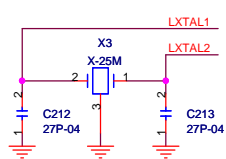
RTL8103EL-GR
01-278-103350

BOM Difference

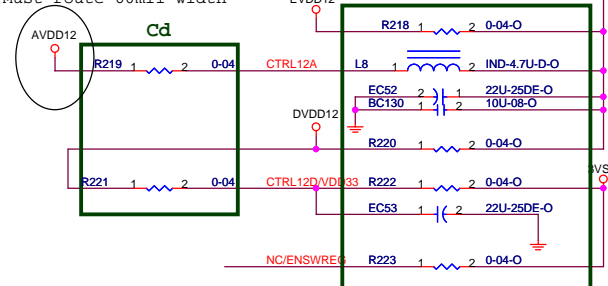
	RTL8111DL-GR 1000M	RTL8103EL-GR 10/100M
Ca	RTL8111DL-GR	RTL8103EL-GR
Cb	X	V
Cc	0-04	.01U-04
Cd	X	V
Ce	V	X
Cf	USBX2-LAN-1000	USBX2-LAN-100

Power Difference

	RTL8111D	RTL8103E
AVDD33 VDD33	3.3V 3VSB供應	3.3V 3VSB供應
CTRL12A	Switching Output	1.2V pinself 供應
DVDD12	1.2V CTRL12A供應	1.2V pinself 供應
EVDD12	1.2V CTRL12A供應	1.2V pinself 供應



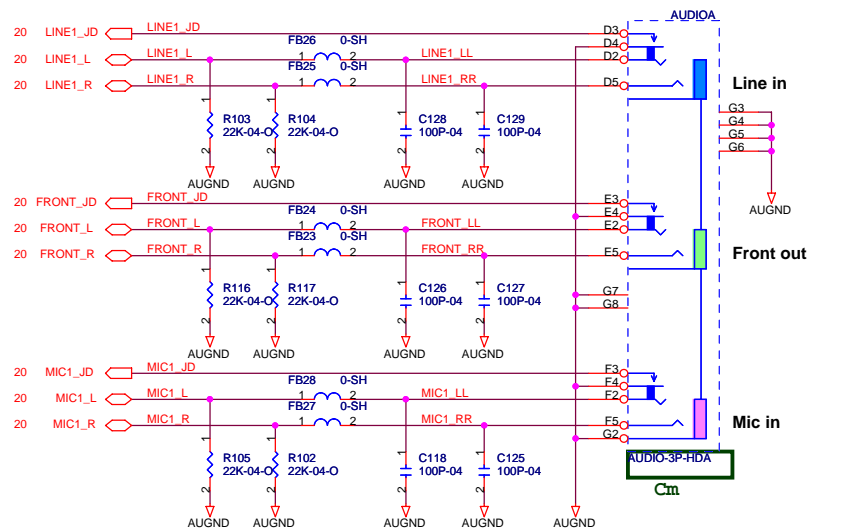
L_L1 & L_R9 place at pin48 with 200mil distance
L_EC1 place at near L_L1
Must route 60mil width



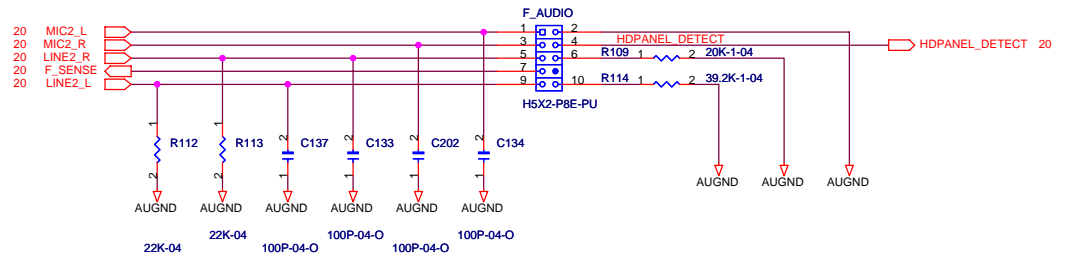
Choke near pin48,
E/C cap near Choke



REAR-AUDIO



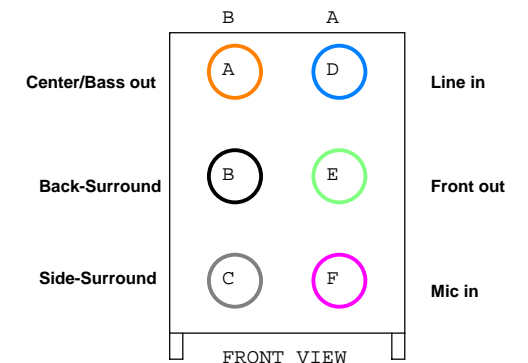
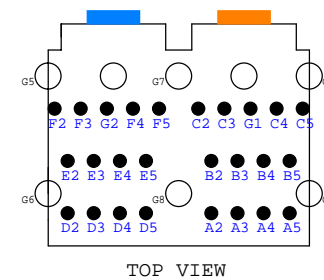
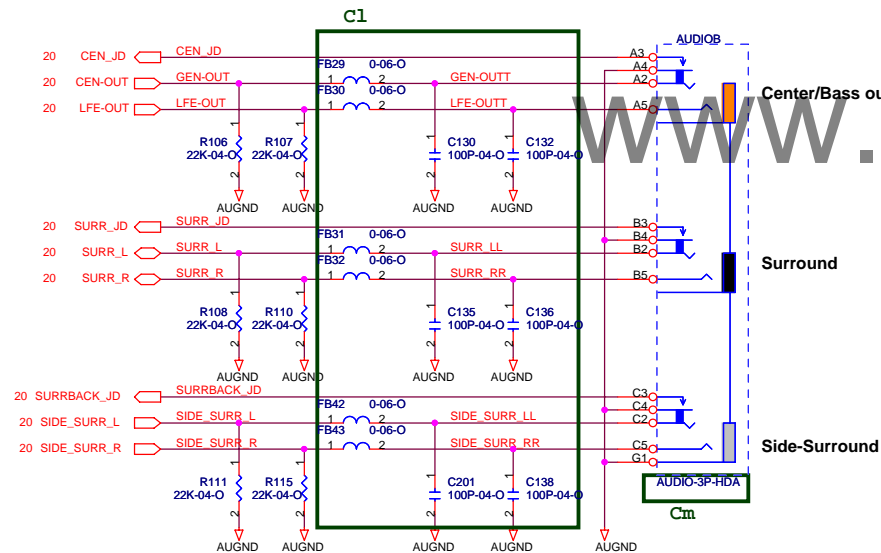
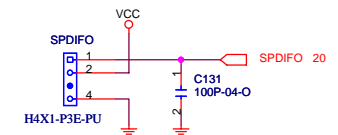
FRONT-AUDIO



CD_IN



SPDIF-OUT



PCB Impedance control			
Impedance (ohm)	Trace Width (mil) (S/W/S)	Trace Length (inch)	Pre-preg
60	5 (20/5/20)	6	2116
50	4 (50/4/50)	6	1080
42	6 (50/6/50)	6	1080

1)Circuit type 1

Layer 1:TOP

Layer 2:PWR

Layer 3:GND

Layer 4:BOTTOM

VCC

JP4

1

2

3

4

J2X2_IP

Trace on layer 1

IMPEDANCE T

IMPEDANCE B

Trace on layer 4

For 104

SPI_ROM_D(104)

SPI-ROM-D-8M

BT(104)

CR2032

CLR_CMOS(1-2)

JP-R

USBPWR_R(1-2)

JP-Y

USBPWR_F(1-2)

JP-Y

NB(104)

HS-38X36X25-SL

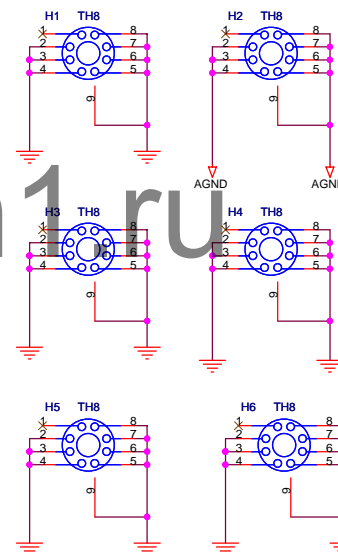
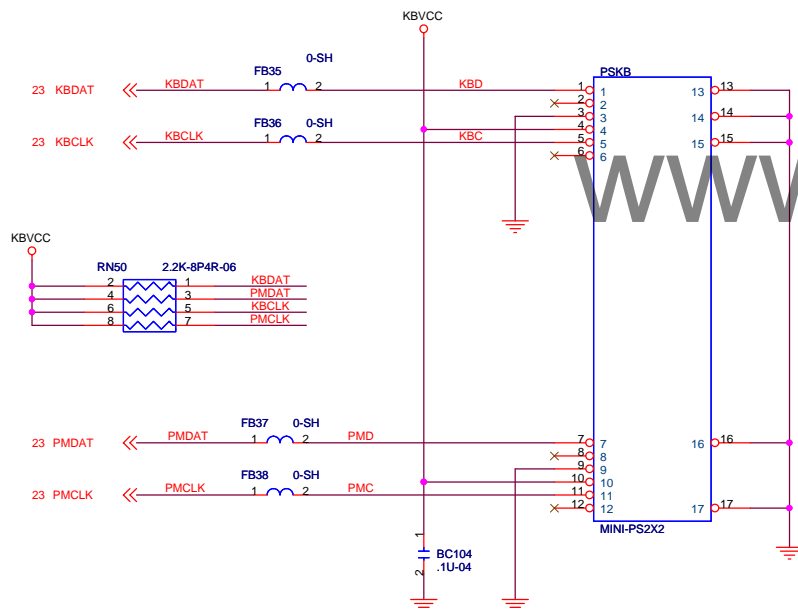
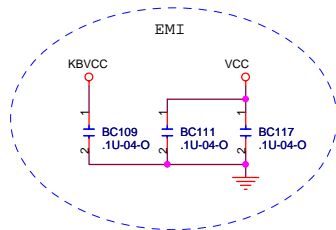
If need 25mm hight :
20-120-010937 or 20-120-011420

For 103

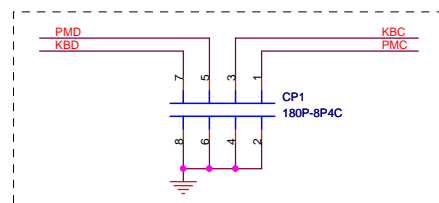
X1(wire)

JP-WI-P6.25

www.aitech1.ru

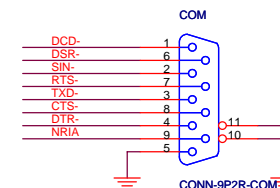
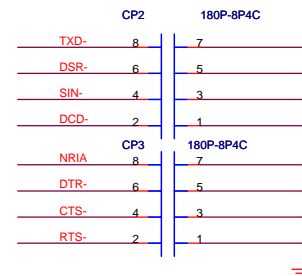
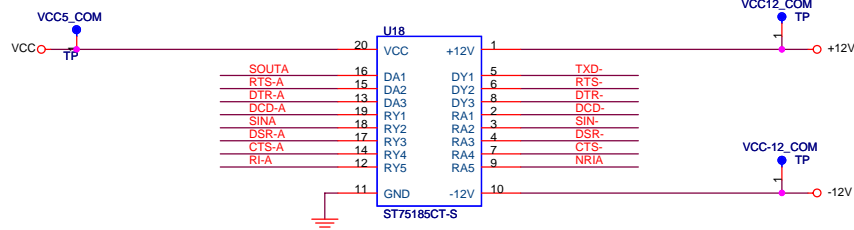


PLACE NEAR CONNECTOR

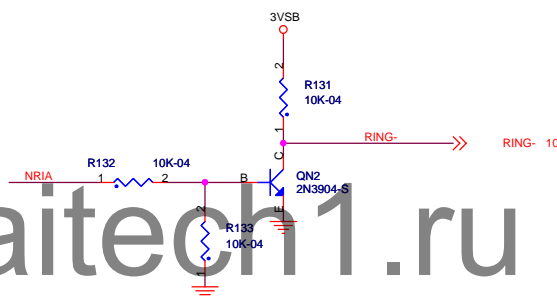


COM Port

23	DCD-A	DCD-A
23	RI-A	RI-A
23	CTS-A	CTS-A
23	DTR-A	DTR-A
23	RTS-A	RTS-A
23	DSR-A	DSR-A
23	SOUTA	SOUTA
23	SINA	SINA

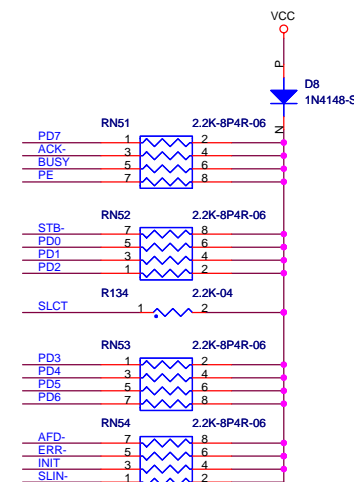
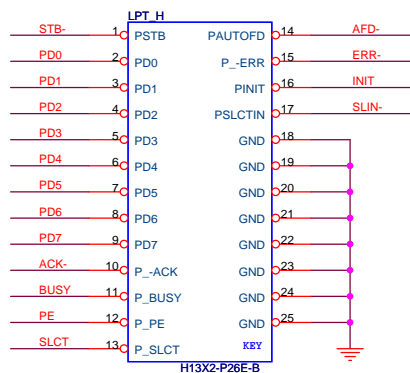
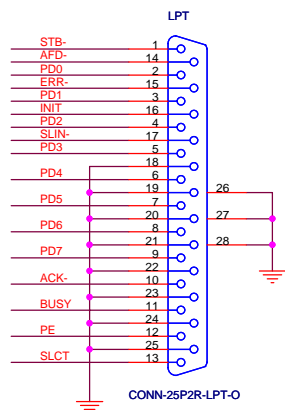


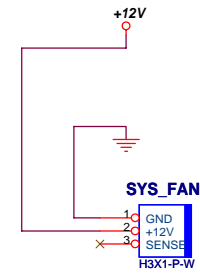
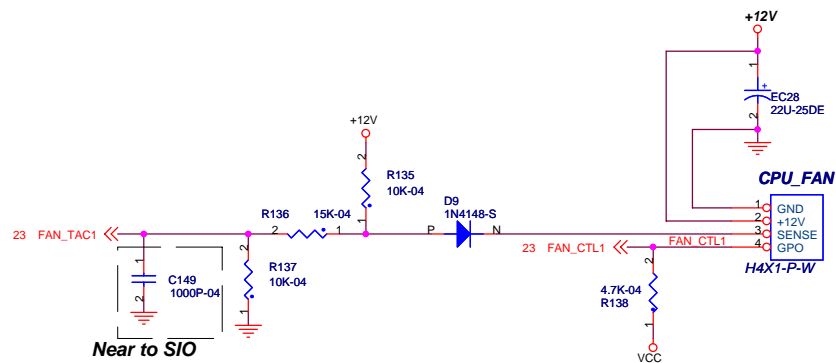
www.aitech1.ru



LPT

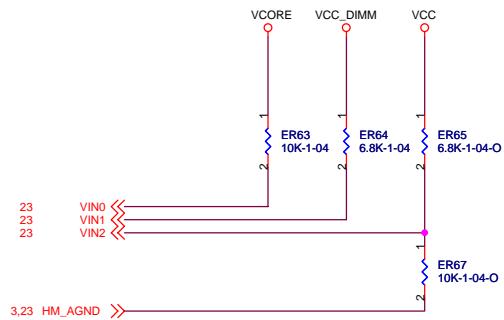
23	STB- << STB-	23	PD[0..7] << PD[0..7]
23	ACK- << ACK-	23	AFD- << AFD-
23	BUSY << BUSY	23	ERR- << ERR-
23	PE << PE	23	INIT << INIT
23	SLCT << SLCT	23	SLIN- << SLIN-





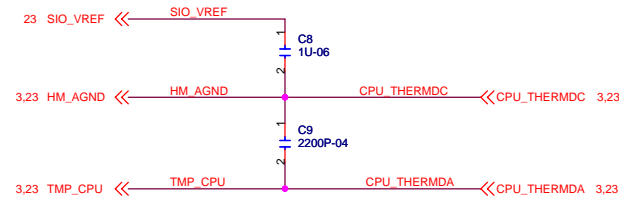
www.aitech1.ru

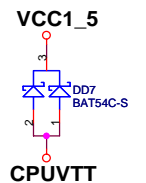
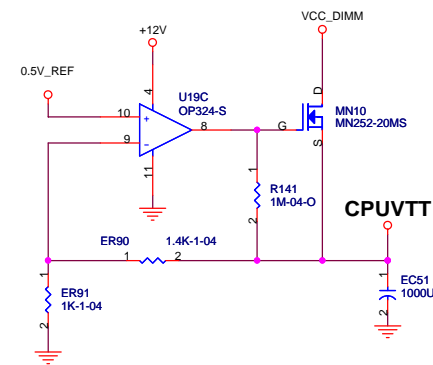
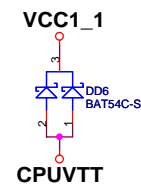
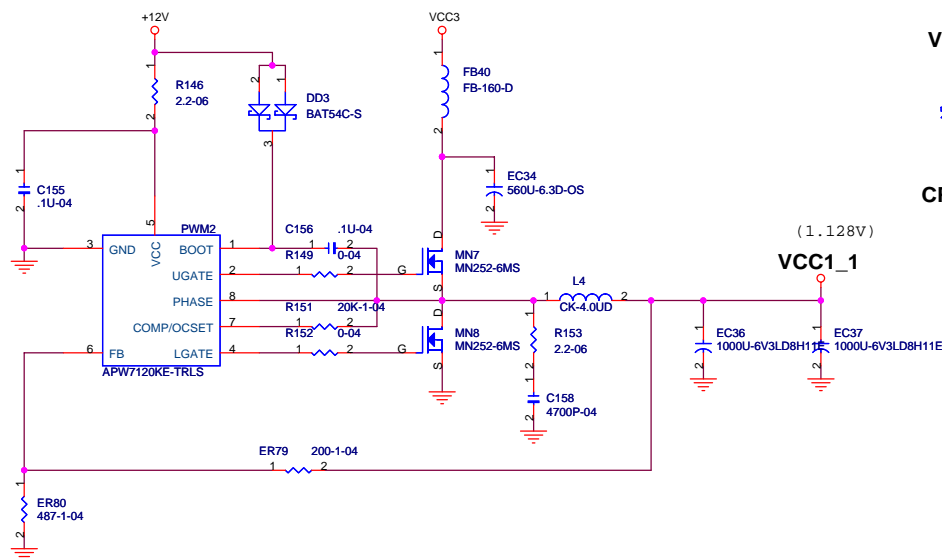
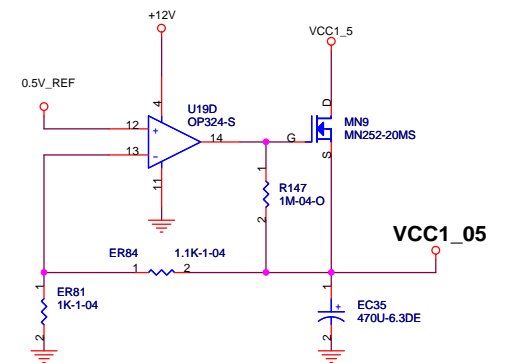
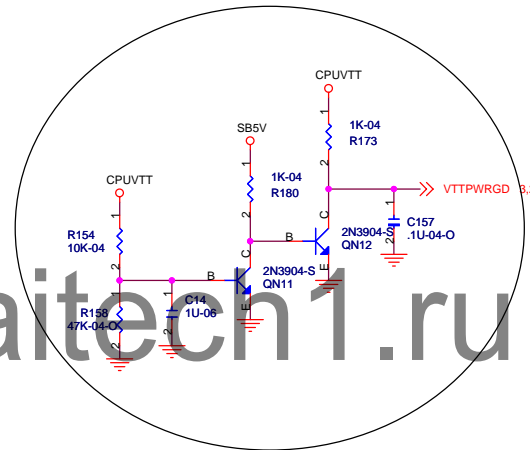
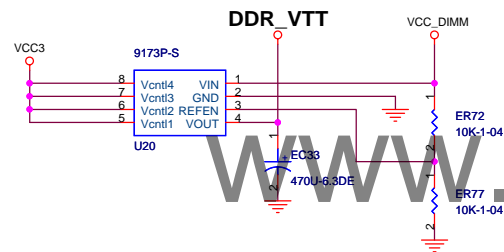
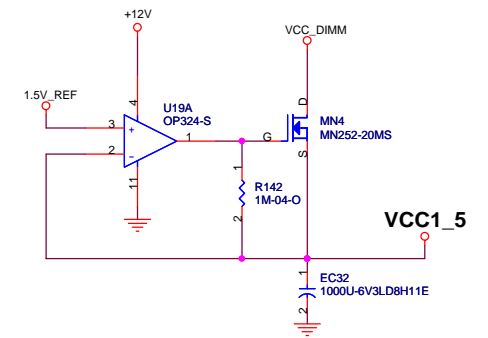
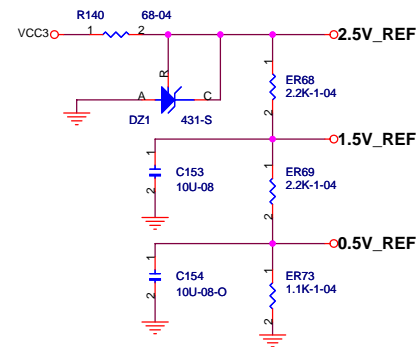
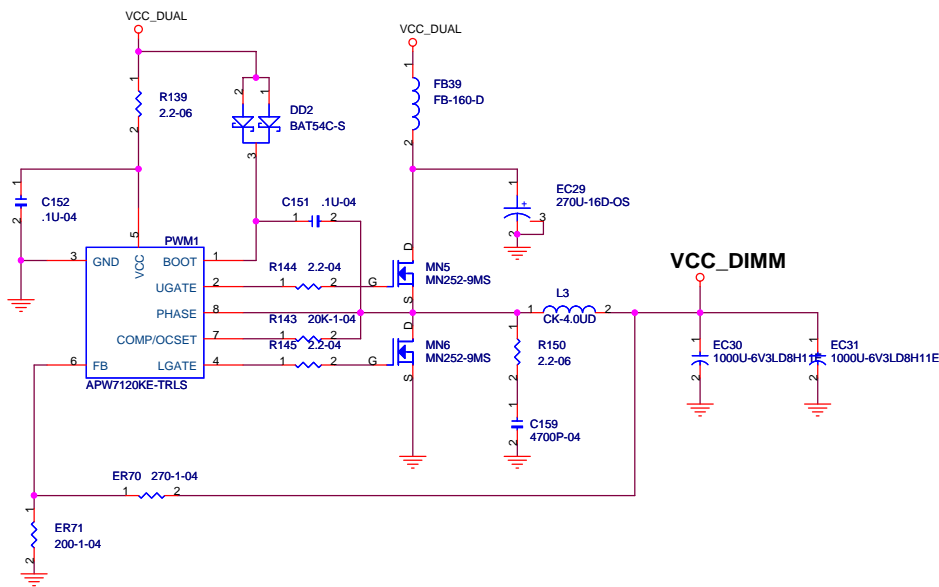
Voltage Monitor

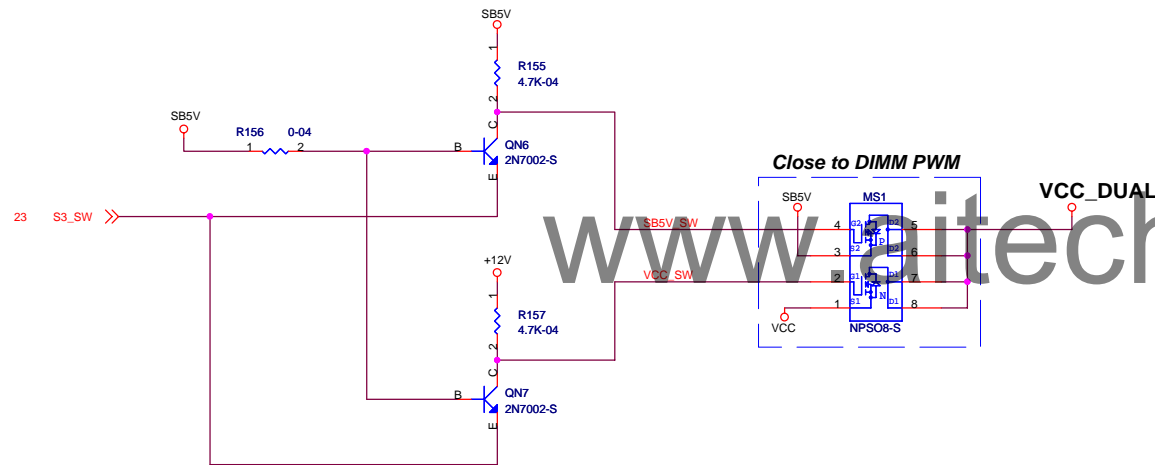
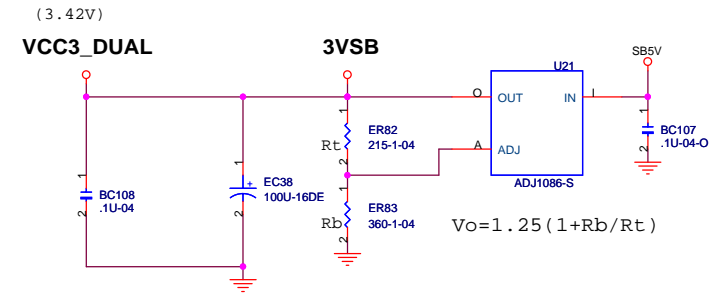
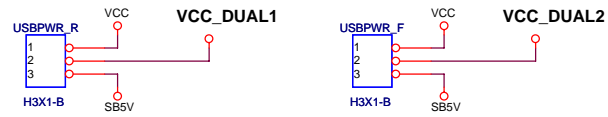


Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode







Memory Power Output Control

	VCC_DUAL	ATX_PWOK	SLP_S4-	SLP_S3-	S3_SW
S0	VCC	1	1	1	1
S1	VCC	1	1	1	1
S3	SB5V	0	1	0	0
S4	0	0	0	0	1
S5	0	0	0	0	1

